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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/650,604	08/30/2000	Thomas J. Krutsick	5	9105

7590 10/24/2006

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EXAMINER	
SEFER, AHMED N	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/650,604	KRUTSICK, THOMAS J.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. In view of the appeal brief filed on 10/14/04, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 11/15/04 was filed after the mailing date of the final Office action on 4/6/04. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 40 and 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 40 and 41 recite the limitation "the method of claim ...". Since both claims 28 and 35 on which claims 40 and 41 depend respectively are drawn to device, there is insufficient antecedent basis for this limitation in the claims.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 28-30, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo ("Kondo") USPN 4,609,935 in view of Gardner ("Gardner") GB 2016208 (of record).

Kondo discloses (see figs. 6-10 and col. 6, lines 46-49) an integrated circuit having a field-plated resistor, the field-plated resistor comprising a resistor body 35 formed in a semiconductor substrate, the resistor body having first and second contact regions; a first insulating layer 33 over the resistor body, the first insulating layer approximately coextensive with the resistor body and having a top surface and a bottom surface; a contact window in the first insulating layer (not shown) and extending from the top surface of the first insulating layer through the first insulating layer through the first insulating layer to the resistor body; a field plate 39 comprising polysilicon (as in claim 29) on the first insulating layer and approximately

coextensive therewith and with the resistor body, the field plate having a top surface and a bottom surface; a second insulating layer 42, with a first portion of the second insulating covering the field plate, an electrical contact to the top surface of the field plate; an electrical contact to the second contact region of the resistor, and electrically insulated from the field plate by oxide layer 38 and a plurality metal conductors 44 formed on the first portion of the second insulating layer, but omits a portion of the bottom surface of the field plate extending through the contact window

Gardner discloses in figs. 1 and 2 a field plate 15 with a portion of the bottom surface extending through a contact window 21 in an insulating layer 16/17 and into contact with a contact region 13 of a resistor 11.

Since Kondo and Gardner are both from the same field of endeavor, resistive elements, the teaching disclosed by Gardner would have been recognized in the pertinent art of Kondo. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Gardner's teachings with Kondo's device, since that would suppress the tendency of the semiconductor surface to deplete or even invert with respect to surface charge as taught by Gardner.

Regarding claim 30, Kondo discloses first and second insulating oxide layers.

Regarding claims 33 and 34, Kondo discloses a barrier layer 41.

7. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo in view of Gardner as applied to claims 28 and 29 above, and further in view of Davis et al. ("Davis") USPN 5,200,733.

The combined references disclose the device structure as recited in the claim, but do not disclose an insulative spacer formed around a field plate.

Davis discloses in fig. 11 an insulative spacer 40 around a field plate.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ an insulative spacer around a field plate, since that would provide the field plate an excellent insulation.

8. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo in view of Gardner.

Kondo discloses (see figs. 6-10 and col. 6, lines 46-49) an integrated circuit having a field-plated resistor, the field-plated resistor comprising a resistor body 35 formed in a semiconductor substrate, the resistor body having first and second contact regions; a first insulating layer 33 over the resistor body, the first insulating layer approximately coextensive with the resistor body and having a top surface and a bottom surface; a contact window in the first insulating layer (not shown) and extending from the top surface of the first insulating layer through the first insulating layer through the first insulating layer to the resistor body; a field plate 39 on the first insulating layer and approximately coextensive therewith and with the resistor body, the field plate having a top surface and a bottom surface; a second insulating layer 42, with a first portion of the second insulating covering the field plate, a metal layer comprising an electrical contact to the top surface of the field plate, an electrical contact to the second contact region of the resistor, and electrically insulated from the field plate by oxide layer 38 and a plurality metal conductors 44 formed on the first portion of the second insulating layer, but omits a portion of the bottom surface of the field plate extending through the contact window.

Gardner discloses in figs. 1 and 2 a field plate 15 with a portion of the bottom surface extending through a contact window 21 in an insulating layer 16/17 and into contact with a contact region 13 of a resistor 11.

Since Kondo and Gardner are both from the same field of endeavor, resistive elements, the teaching disclosed by Gardner would have been recognized in the pertinent art of Kondo. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Gardner's teachings with Kondo's device, since that would suppress the tendency of the semiconductor surface to deplete or even invert with respect to surface charge as taught by Gardner.

9. Claims 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo in view of Gardner.

Kondo discloses (see figs. 4-10 and col. 6, lines 46-49) a method of the manufacture of an integrated circuit having a field-plated resistor, the field-plated resistor comprising forming a resistor body 35 in a semiconductor substrate, the resistor body having first and second contact regions; a first insulating layer 33 over the resistor body, the first insulating layer approximately coextensive with the resistor body and having a top surface and a bottom surface; forming a contact window in the first insulating layer (not shown) and extending from the top surface of the first insulating layer through the first insulating layer through the first insulating layer to the resistor body; forming a field plate 39 comprising polysilicon (as in claim 37) on the first insulating layer and approximately coextensive therewith and with the resistor body, the field plate having a top surface and a bottom surface; depositing a second insulating layer 42, with a first portion of the second insulating covering the field plate; depositing a metal layer comprising

an electrical contact to the top surface of the field plate, an electrical contact to the second contact region of the resistor, and electrically insulated from the field plate by oxide layer 38 and a plurality metal conductors 44 formed on the first portion of the second insulating layer, but omits a portion of the bottom surface of the field plate extending through the contact window.

Gardner discloses in figs. 1 and 2 a field plate 15 with a portion of the bottom surface extending through a contact window 21 in an insulating layer 16/17 and into contact with a contact region 13 of a resistor 11.

Since Kondo and Gardner are both from the same field of endeavor, resistive elements, the teaching disclosed by Gardner would have been recognized in the pertinent art of Kondo. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Gardner's teachings with Kondo's device, since that would suppress the tendency of the semiconductor surface to deplete or even invert with respect to surface charge as taught by Gardner.

Regarding claim 38, Kondo discloses first and second insulating oxide layers.

10. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo in view of Gardner as applied to claims 36 and 38 above, and further in view of Davis.

The combined references disclose the device structure as recited in the claim, but do not disclose an insulative spacer formed around a field plate.

Davis discloses in fig. 11 an insulative spacer 40 around a field plate.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ an insulative spacer around a field plate, since that would provide the field plate an excellent insulation.

Allowable Subject Matter

11. Claim 42 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. Claims 40 and 41 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
October 12, 2006

LEONARDO ANDUJA
PRIMARY EXAMINER